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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,110	KINSMAN, LARRY D.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/10/2004 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 14-16, 18, 20, 37-39, and 54-55** are rejected under 35 U.S.C. 102(e) as being anticipated by Okada et al. U.S. Patent Application Publication 2004/0188838 (the '838 publication).

The '838 publication discloses in Figures 13's and 15's, and respective portions of the specification a device and method as claimed.

Referring to **claim 1**, the '838 publication discloses a semiconductor module, comprising:

a dielectric flex tape substrate (45B,D, paragraph [0095]) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads (no number) on the first tape surface, and a plurality of traces (not shown), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (22A) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (37) on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 37** and using the same reference characters and citations as detailed above for claim 1 where applicable, the '838 publication discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claim 55**, the '838 publication further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claims 14 and 54**, the '838 publication further discloses an encapsulant (38,24) applied to the electrical connections between the die attach pads and the respective tape terminal pads.

Referring to **claim 15**, the '838 publication further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claim 38**, the '838 publication further discloses that the tape substrate is attached to the first surface of the semiconductor die.

Referring to **claim 16**, the '838 publication further discloses that the electrical connections are made using solder bumps.

Referring to **claim 39**, the '838 publication further discloses that the electrical connections are formed by solder bumps.

Referring to **claim 18**, the '838 publication further discloses that the electrical connections are made using tape automated bonding (paragraph [0105]).

Referring to **claim 20**, the '838 publication further discloses an encapsulant underfill (38) applied to the electrical connections between the die attach pads and the respective tape terminal pads.

3. **Claims 1-2, 5-6, 13, 15-16, 18, 37-38, 42, 45, 47, and 55** are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. U.S. Patent Application Publication 2003/0201447 (the '447 publication).

The '447 publication discloses in Figures 9's and 10's, and respective portions of the specification a device and method as claimed.

Referring to **claim 1**, the '447 publication discloses a semiconductor module, comprising:

a dielectric flex tape substrate (FPC 909 – "flexible printed circuit", paragraph [0162]) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads (no number) on the first tape surface, and a plurality of traces (not labeled), each trace electrically

connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (generally represented by 901, 902, and semiconductor substrate 910, paragraph [0149]) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (no number, through which the semiconductor die is to be electrically connected to the FPC 909) on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads (as is evident by Fig. 9B).

Referring to independent **claim 37** and using the same reference characters and citations as detailed above for claim 1 where applicable, the '447 publication discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claim 55**, the '447 publication further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claims 2 and 42**, the '447 publication further discloses that the semiconductor die contains an array (901, 902) of pixels.

Referring to **claims 5 and 45**, the '447 publication further discloses that the pixel array includes CMOS pixels (paragraph [0158]).

Referring to **claims 6 and 47**, the '447 publication further discloses a cover glass (904) over the pixel array.

Referring to **claim 13**, the '447 publication further discloses that the edge is an only one of a plurality of edges having die attach pads (as is evident by Fig. 9A).

Referring to **claim 15**, the '447 publication further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claim 38**, the '447 publication further discloses that the tape substrate is attached to the first surface of the semiconductor die.

Referring to **claims 16 and 18**, the '447 publication further discloses that the electrical connections are made using tape automated bonding (paragraph [0003]).

4. **Claims 1-4, 6-7, 9-12, 14-16, 19, 21-24, 29, 37-44, 47-48, and 52-55** are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. U.S. Patent 6,768,516 (the '516 patent, and priority is based on patent application publication date of publication 2001/0050717).

The '516 patent discloses in the figures, particularly Figure 12, and respective portions of the specification a device and method as claimed.

Referring to **claim 1**, the '516 patent discloses a semiconductor module, comprising:

a dielectric flex tape substrate (5, column 4, line 37) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads (no number) on the first tape surface, and a plurality of traces (not labeled), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (4 or stacked die 4/9) having a first die surface (the upper surface of element 4 of stacked die 4/9 or the lower surface of element 9 of stacked die 4/9), a second die surface (opposite to the first surface), an edge, and a plurality of die attach pads (27 of semiconductor die 4, for example Fig. 14, or not-shown-no-labeled pads of semiconductor die 9 of fig. 14, which pads are inherent for bonding wires 42 to be bonded to) on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 23** and using the same reference characters and citations as detailed above for claim 1 where applicable, the '516 patent discloses a camera module, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array (no detail is disclosed explicitly, but, at the time the invention was made, the semiconductor die must comprise a pixel array to function electrically, optically, and economically), a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the semiconductor die being

attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure (2/3) disposed over the pixel array.

Referring to independent **claim 37** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '516 patent discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claim 55**, the '516 patent further discloses that the tape substrate partially overlaps the first die (4) surface.

Referring to **claims 2 and 42**, the '516 patent's semiconductor die, as detailed above, inherently contains an array of pixels.

Referring to **claims 3-4 and 43-44**, the '516 patent further discloses a lens structure (generally referred to as 2/3) disposed over and on the array of pixels (as noted above, the semiconductor die inherently comprises an array of pixels, and since the lens structure is

disposed over and on the semiconductor die, the lens structure is disposed over and on the array of pixels).

Referring to **claims 6-7 and 47-48**, the '516 patent further discloses a cover glass (24) over the pixel array and that the cover glass is an infrared cut filter (column 4, lines 11-12).

Referring to **claim 24**, the '516 patent further discloses a cover glass (24) disposed between the lens structure (2/3) and the pixel array.

Referring to **claim 29**, the '516 patent further discloses that an infrared lens (column 4, lines 11-12) formed over said semiconductor die.

Referring to **claims 9 and 50**, the '516 patent further discloses a lens structure (2/3) disposed over the cover glass (24).

Referring to **claims 10-12 and 51-53**, the '516 patent further discloses a lens holder (3) disposed over and on ("on" is interpreted broadly) the cover glass and on the (inherent) pixel array.

Referring to **claims 14 and 54**, the '516 patent further discloses an encapsulant (43,44) applied to the electrical connections between the die attach pads adjacent the edge of the die and the respective tape terminal pads on the first tape surface near the end of the tape substrate.

Referring to **claim 15**, the '516 patent further discloses that the tape substrate partially overlaps the first die (4) surface.

Referring to **claim 38**, the '516 patent further discloses that the tape substrate (5) is attached to the first surface of the semiconductor die (4, Fig. 12).

Referring to **claims 16 and 39**, although not explicitly disclosed, bumps 27 are solder bumps and that the electrical connections are made using solder bumps.

Referring to **claim 19**, the '516 patent further discloses that the electrical connections are made using anisotropic conductive film (column 5, last paragraph).

Referring to **claim 21**, the '516 patent further discloses that the tape substrate (5) at least partially overlaps the second die surface (the lower surface of semiconductor die 9 of the stacked die 4/9 of Fig. 2; or the lower surface of die 4 of Fig. 20; or the upper surface of the semiconductor die 4 of the stacked die 4/9 of Fig. 14).

Referring to **claim 40**, the '516 patent further discloses that the tape substrate (5) is attached to the second surface of the semiconductor die (the lower surface of semiconductor die 9 of the stacked die 4/9 of Fig. 2; or the lower surface of die 4 of Fig. 20; or the upper surface of the semiconductor die 4 of the stacked die 4/9 of Fig. 14).

Referring to **claims 22 and 41**, the '516 patent further discloses that the electrical connections (between the die attach pads (not-shown-no-labeled pads of semiconductor die 9 of fig. 14, which pads are inherent for bonding wires 42 to be bonded to, on the first die surface adjacent the edge) and respective tape terminal pads) are formed by wire bonds (6, Fig. 20 or 42 of Fig. 14).

5. **Claims 1-4, 6, 8-12, 15, 23-24, 26, 30-31, 33, 37-38, 42-44, 46-47, 49-53, and 55** are rejected under 35 U.S.C. 102(b) as being anticipated by Kimba et al. U.S. Patent 6,528,778 (the '778 patent).

The '778 patent discloses in the figures, particularly Figures 4B and 6B, and respective portions of the specification a device and method as claimed.

Referring to **claim 1**, the '778 patent discloses a semiconductor module, comprising:

a dielectric flex tape substrate (23, column 4, line 27) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads (no number) on the first tape surface, and a plurality of traces (not shown), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (21) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (generally referred to as 25, Fig. 2B) on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 23** and using the same reference characters and citations as detailed above for claim 1 where applicable, the '778 patent discloses a camera module, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array (column 4, lines 28-35), a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure (5/10) disposed over the pixel array.

Referring to independent **claim 30** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '778 patent discloses an imaging apparatus comprising:

a processor (not shown but must be present for the device to function, column 4, lines 43-45: "the optical unit 1 serving as the AF sensor can *output* a defocus quantity which is used for *controlling* a position of a taking lens of the camera", emphasis added); and

a camera module electrically connected to the processor, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array, a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure disposed over the pixel array.

Referring to independent **claim 37** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '778 patent discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claim 55**, the '778 patent further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claims 2 and 42**, the '778 patent's semiconductor die, as detailed above, inherently contains an array of pixels.

Referring to **claims 3-4 and 43-44**, the '778 patent further discloses a lens structure (generally referred to as 5/10) disposed over and on the array of pixels.

Referring to **claims 6 and 47**, the '778 patent further discloses a cover glass (22, "transparent plate", column 4, lines 26-27) over the pixel array.

Referring to **claims 8 and 49**, the '778 patent further discloses that the cover glass (22) is adhered directly to the die (21, as is evident from the figures).

Referring to **claims 24 and 31**, the '778 patent further discloses a cover glass (22) disposed between the lens structure (5/10) and the pixel array.

Referring to **claims 9 and 50**, the '778 patent further discloses a lens structure (5/10) disposed over the cover glass (22).

Referring to **claims 10-12 and 51-53**, the '778 patent further discloses a lens holder (10) disposed over and on the cover glass (22) and on the pixel array.

Referring to **claim 15**, the '778 patent further discloses that the tape substrate (23) partially overlaps the first die surface.

Referring to **claim 38**, the '778 patent further discloses that the tape substrate (23) is attached to the first surface of the semiconductor die (21).

Referring to **claims 26, 33, and 46**, the '778 patent further discloses that the pixel array includes CCD pixels (column 4, lines 28-35).

6. **Claims 1-5, 12-13, 15-17, 23, 25-26, 28, 30, 32-33, 35, 37-39, 42-45, 53, and 55** are rejected under 35 U.S.C. 102(b) as being anticipated by Takiar et al. U.S. Patent 6,384,397 (the '397 patent).

The '397 patent discloses in Figures 2 and 8 through 11, particularly Figure 9, and respective portions of the specification a device and method as claimed.

Referring to **claim 1**, the '397 patent discloses a semiconductor module, comprising:

a dielectric flex tape substrate (77, Fig. 9, column 7, first full paragraph) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads (78) on the first tape surface, and a plurality of traces (not shown), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die ("sensor package" 32, column 7, lines 1 and 18-22, and column 5, last full paragraph) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (76) on the first die surface adjacent ("adjacent" is interpreted broadly to compensate for the fact that the figures are probably not drawn to true scale) the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 23** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the '397 patent discloses a camera module, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array ("CMOS or CCD sensor device", column 7, lines 1 and 18-22, and column 5, last full paragraph, and it should be apparent, as shown by other references of record, that these devices are arrayed in pixels), a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure (35/31) disposed over the pixel array.

Referring to independent **claim 30** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '397 patent discloses an imaging apparatus comprising:

a processor (not shown but must be present for the device to function, column 1, lines 25-37: "The imaging sensor is connected to a printed circuit board in order to be *electrically connected to the rest of the imaging system*", emphasis added); and

a camera module electrically connected to the processor, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array, a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the

semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure disposed over the pixel array.

Referring to independent **claim 37** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '397 patent discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claim 55**, the '397 patent further discloses that the tape substrate partially overlaps the first die surface.

Referring to **claims 2 and 42**, the '397 patent's semiconductor die, as detailed above, inherently contains an array of pixels.

Referring to **claims 3-4 and 43-44**, the '397 patent further discloses, as noted above, a lens structure (35/31) disposed over and on the array of pixels.

Referring to **claims 5, 25, 32, and 45**, the '397 patent further discloses that, as detailed above, the pixel array includes CMOS pixels.

Referring to **claims 12 and 53**, the '397 patent further discloses a lens holder (35, "lens housing") disposed over the pixel array.

Referring to **claim 13**, the '397 patent further discloses that the edge is an only one of a plurality of edges having die attach pads (Figs. 9 and 10).

Referring to **claim 15**, the '397 patent further discloses that the tape substrate (77) partially overlaps the first die surface.

Referring to **claim 38**, the '397 patent further discloses that the tape substrate (77) is attached to the first surface of the semiconductor die (21).

Referring to **claims 16, 28, 35, and 39**, the '397 patent further discloses that the electrical connections are made using solder bumps (column 7, first paragraph).

Referring to **claim 17,** the '397 patent further discloses that the electrical connections are made by using a reflow process (column 7, first paragraph).

Referring to **claims 26, 33, and 46**, the '397 patent further discloses that the pixel array, as noted above, includes CCD pixels (column 7, lines 18-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 5, 25, 30-32, 36, and 45** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '516 patent.

Referring to **claim 30**, the '516 patent discloses a device as claimed and as detailed above for claims 1, 23, and 37, including a camera module 20 and a processor 9 (image processing chip). The difference between the '516 patent's device and that of the claimed is that the processor is integral to the camera module in the case of the '516 patent and the processor is electrically connected to the camera module as claimed. Nevertheless, since Applicant has failed to disclose an advantage of one design over the other, the change from one design to the other would have been obvious to one of ordinary skill in the art at the time the invention was made. It is noted that the improvement of the '516 patent over the prior art is to integrate the processor to the camera module; however, the issue here is the obviousness of the different designs to one of ordinary skill in the art.

Referring to **claims 5, 25, 32, and 45**, since the '516 patent discloses a CMOS camera module, it appear that that the inherent (as noted above) pixel array includes CMOS pixels.

Referring to **claim 31**, the '516 patent further discloses a cover glass (24) disposed between the lens structure (2/3) and the pixel array.

Referring to **claim 36**, the '516 patent further discloses that an infrared lens (column 4, lines 11-12) formed over said semiconductor die.

8. **Claims 6, 8-11, 24, 31, 47, and 49-52** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '397 patent.

Referring to **claims 6, 24, 31, and 47**, the '397 patent discloses in Fig. 9 a device and an inherent method of forming the device as claimed and as detailed above for claims 1, 23, 30, and 37, including the lens structure 35/31 comprising a lens holder 35 ("lens housing") and lens 31

and the CMOS-or-CCD semiconductor die 32 comprising the inherent pixel array, but fails to disclose in this embodiment a cover glass. Thus the reference further fails to disclose, for this embodiment, that the cover glass is formed between the lens structure and the pixel array, that the cover glass is adhered directly to the die (in reference to claims 8 and 49), that the lens structure is disposed over the cover glass (claims 9 and 50), and that the lens holder (35) is disposed over and on the cover glass and on the pixel array (claims 10-11 and 51-52).

However, in the embodiments of Fig. 8 and Fig. 2, the '397 patent teaches that to protect the semiconductor die from dust particles, moistures, etc., a plate of glass 20 is attached (column 1, lines 50-57). Specifically, the reference discloses in Figs. 2 and 8 that the cover glass is formed between the lens structure and the pixel array, that the cover glass is adhered directly to the die, that the lens structure is disposed over the cover glass, and that the lens holder is disposed over and on the cover glass and on the pixel array.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Fig. 9 to include a cover glass. One would have been motivated to make such a modification in view of the teachings in Figs. 2 and 8 that such a cover glass protects the semiconductor die from dust particles, moistures, etc.

9. **Claims 1, 21-22, 37, and 40-41** are rejected under 35 U.S.C. §103(a) as being unpatentable over Tamura et al. U.S. Patent Application Publication 2004/0027477 (the '477 publication).

The '477 publication discloses in Figures 1's and 7's and respective portions of the specification a device and method substantially as claimed. The difference between the

reference and the claims is the process by which the semiconductor die is attached to the dielectric flex tape.

Referring to **claim 1**, the '477 publication discloses a semiconductor module, comprising:

a dielectric flex tape substrate (11, paragraph [0061]) having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads ("connection electrodes" 11c, Fig. 7A, paragraph [0087]) on the first tape surface, and a plurality of traces (11E), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (22) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (no number) on the first die surface adjacent the edge, the semiconductor die, together with the assembly 20, being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 37** and using the same reference characters and citations and interpretations as detailed above for claim 1 where applicable, the '477 publication discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the assembly 20, the assembly including semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

The difference between the reference's and the claims' device, i.e., "the semiconductor die, together with the assembly 20, being attached to and overlapping the end of the tape substrate" and "the semiconductor die being attached to and overlapping the end of the tape substrate", does not result in a difference in the end products, i.e., to form electrical connections between the semiconductor die and the tape substrate, and therefore the difference, and hence the change, would have been obvious to one of ordinary skill in the art at the time the invention was made.

Referring to claims 21-22 and 40-41, the tape substrate 11 of the thus changed device and method of the '477 publication at least partially overlaps the second die surface (the second die surface is opposite to the first die surface), and wherein the electrical connections are made (partly) using wire bonding.

Claim Rejections § 102 & § 103

10. Claims rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kim et al. U.S. Patent Application Publication 2003/0223008 (the '008 publication).

The '477 publication discloses in Figure 4 (Figs. 1-3 for additional details that are missing from Fig. 4) and respective portions of the specification a device and method as claimed or substantially as claimed. The "difference" between the reference and the claims is the dielectric flex tape substrate. Specifically, the claims recite a dielectric flex tape substrate (32), and the

reference discloses a dielectric flex tape substrate (FPCB 26) and a substrate 21. And if one of ordinary skill in the art interprets "dielectric flex tape substrate 26 and substrate 21" broadly as dielectric flex tape substrate 26/21, then the claims are anticipated by the '008 publication; on the other hand, if one of ordinary skill in the art interprets "dielectric flex tape substrate 26 and substrate 21" as different from dielectric flex tape substrate 32, then the claims are obvious over the '008 publication, simply because "dielectric flex tape substrate 26 and substrate 21" and "dielectric flex tape substrate 32" are functionally equivalent. Specifically:

Referring to **claim 1**, the '008 publication discloses a semiconductor module, comprising:

a dielectric flex tape substrate (26/21, paragraph [0034]) having a first tape surface (generally defined by upper surface(s) of element 21 and upper surface(s) of element 26 not covered by element 21), a second tape surface (opposite to the first surface), an end, a plurality of tape terminal pads (not shown) on the first tape surface, and a plurality of traces (not shown), each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate; and

a semiconductor die (22) having a first die surface, a second die surface, an edge, and a plurality of die attach pads (not shown) on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between the die attach pads and respective tape terminal pads.

Referring to independent **claim 23** and using the same reference characters, interpretations, and citations as detailed above for claim 1 where applicable, the '008 publication discloses a camera module, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array (CCD or CMOS image sensor technology – paragraph [0006] – and it shall be apparent from the other references of record that CCD or CMOS image sensor technology inherently comprises CCD or CMOS pixel arrays), a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure (25/27) disposed over the pixel array.

Referring to independent **claim 30** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '008 publication discloses an imaging apparatus comprising:

a processor (ISP 23, "image signal process package", paragraph [0008]); and

a camera module electrically connected to the processor, comprising:

a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface near the end of the tape substrate, and a plurality of traces, each trace electrically connecting to a respective one of the terminal pads;

a semiconductor die having a pixel array, a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge, the

semiconductor die being attached to and overlapping the end of the tape substrate and having electrical connections between die attach pads and respective tape terminal pads; and

a lens structure disposed over the pixel array.

Referring to independent **claim 37** and using the same reference characters and citations and interpretations as detailed above for claims 1 and 23 where applicable, the '008 publication discloses a method of forming a semiconductor die package, said method comprising the acts of:

providing a semiconductor die having a first die surface, a second die surface, an edge, and a plurality of die attach pads on the first die surface adjacent the edge;

attaching a dielectric flex tape substrate having a first tape surface, a second tape surface, an end, a plurality of tape terminal pads on the first tape surface, and a plurality of traces, each trace electrically connecting to a respective one of the tape terminal pads on the first tape surface of the tape substrate to the semiconductor die; and

forming electrical connections between the die attach pads adjacent the edge of the die and respective tape terminal pads on the first tape surface of the tape substrate.

Referring to **claims 2 and 42**, the '008 publication's semiconductor die, as detailed above, inherently contains an array of pixels.

Referring to **claims 3-4 and 43-44**, the '008 publication further discloses a lens structure (generally referred to as 25/27) disposed over and on the array of pixels (as noted above, the semiconductor die inherently comprises an array of pixels, and since the lens structure is disposed over and on the semiconductor die, the lens structure is disposed over and on the array of pixels).

Referring to **claims 5, 25, 32, and 45**, the '008 publication further discloses that, as detailed above, the pixel array includes CMOS pixels.

Referring to **claims 6-7 and 47-48**, the '008 publication further discloses a cover glass (24) over the pixel array and that the cover glass is an infrared cut filter (paragraph [0009], and it shall be apparent that element 24 of Fig. 4 is the same as or substantially the same as element 104 of Fig. 1).

Referring to **claims 24 and 31**, the '008 publication further discloses a cover glass (24) disposed between the lens structure (25/27) and the pixel array.

Referring to **claims 29 and 36**, the '008 publication further discloses that an infrared lens, as noted above, formed over said semiconductor die.

Referring to **claims 9 and 50**, the '008 publication further discloses a lens structure (25/27) disposed over the cover glass (24, "over" is interpreted broadly).

Referring to **claims 10-12 and 51-53**, the '008 publication further discloses a lens holder (25) disposed over and on ("on" and "over" are interpreted broadly) the cover glass and on the (inherent) pixel array.

Referring to **claim 21**, the '008 publication further discloses that the tape substrate (26/21) at least partially overlaps ("to have an area or a range in common with") the second die surface.

Referring to **claim 40**, the '008 publication further discloses that the tape substrate (26/21) is attached to the second surface of the semiconductor die.

Referring to **claims 22, 27, 34, and 41**, the '008 publication further discloses that the electrical connections are formed by wire bonds (no label).

Referring to **claims 26, 33, and 46**, the '008 publication further discloses that the pixel array includes CCD pixels (paragraph [0006]).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
December 29, 2004

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